In the Claims

Claim 1 (original): A method of forming a field-effect transistor on a substrate, said method comprising steps of:

forming a buffer layer on said substrate, said buffer layer comprising ALD silicon dioxide;

forming a high-k dielectric layer over said buffer layer.

Claim 2 (original): The method of claim 1 further comprising a step of forming a gate electrode layer over said high-k dielectric layer.

Claim 3 (original): The method of claim 1 wherein said step of forming said buffer layer comprises utilizing a silicon tetrachloride precursor in an atomic layer deposition process.

Claim 4 (original): The method of claim 1 wherein said buffer layer comprises substantially no pin-hole defects.

Claim 5 (original): The method of claim 1 wherein said buffer layer has a thickness less than approximately 5.0 Angstroms.

Claim 6 (original): The method of claim 2 wherein said gate electrode layer comprises polycrystalline silicon.

Claim 7 (original): The method of claim 1 wherein said high-k dielectric layer is selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.

Claim 8 (original): A method for forming a field effect transistor on a substrate, said method comprising a step of forming a buffer layer on said substrate, said method being characterized by:

forming a high-k dielectric layer on said buffer layer, wherein said buffer layer comprises ALD silicon dioxide.

Claim 9 (original): The method of claim 8 further comprising a step of forming a gate electrode layer over said high-k dielectric layer.

Claim 10 (original): The method of claim 8 wherein said step of forming said buffer layer comprises utilizing a silicon tetrachloride precursor in an atomic layer deposition process.

Claim 11 (original): The method of claim 8 wherein said buffer layer comprises substantially no pin-hole defects.

Claim 12 (original): The method of claim 8 wherein said buffer layer has a thickness less than approximately 5.0 Angstroms.

Claim 13 (original): The method of claim 9 wherein said gate electrode layer comprises polycrystalline silicon.

Claim 14 (original): The method of claim 8 wherein said high-k dielectric layer is selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.

Claims 15-20 (canceled).